Simulation of CMOS technology microcircuit elements with eco-friendly practices in agro-industrial production

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Abstract. The paper explores contemporary design technologies for CMOS LSIs and examines challenges encountered during the modelling of LSIs at various hierarchical levels within the design process. The analysis underscores the pressing need for developing software tools for fault modelling while minimizing computational expenses. In addition to addressing the technical aspects, this study sheds light on the influence of ecology and agro-industrial practices on the microcircuit modelling process. Emphasis is placed on resource efficiency and mitigating adverse environmental impacts, particularly in the context of agro-industrial production. The paper discusses the requirements for creating and utilizing SF block libraries, aiming at establishing databases facilitating swift identification, environmental monitoring, and evaluation of the ecological footprint resulting from agro-industrial activities. Moreover, the paper presents principles for constructing VLSI CAD centres that navigate the delicate balance between advanced technologies and environmental sustainability. These principles provide a foundation for developing a unified hardware and software complex tailored for designing radio-electronic equipment while taking into consideration the specific needs and challenges of the agricultural sector.

1 Introduction

In electronics, the most knowledge-intensive procedures, rich in complex mathematical software, are VLSI design procedures. To a large extent, methods, algorithms, and languages focused on VLSI design can also be used in the design of radio-electronic devices, in which microcircuits form the element base [1].

VLSI design is multi-level, with each level characterized by its own mathematical software used for modeling and analysis of circuits.

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Currently, for designing LSIs, both the traditional and the so-called “separation of functions” technology are used, when the design and manufacture of LSIs is carried out by different enterprises [2-4]. In both cases, a top-down design approach is used.

With this method, design begins from the top level - behavioral modeling, then moves on to functional-logical, circuit-technical, topological and design of photomasks and manufacturing of LSIs. At the behavioral level, they operate with algorithms to be implemented in VLSI, which, as a rule, are presented in hardware design languages

In functional design, there are system, register (level of register transfers), logical, circuit, and component (device technology) levels. Often the register and logical levels are combined into a functional-logical level, at which the requirements for functional and circuit characteristics are formulated, the general characteristics of VLSI construction are determined, and operational and control blocks are identified. They create a schedule of operations for a given algorithm, i.e. distribute operations across time clocks and functional blocks, ensuring parallelization and pipelineization of operations implemented in VLSI.

When using the “separation of functions” technology, the design process goes through the same stages, but the design and manufacturing stage can be carried out by different enterprises.

As a rule, each large electronic enterprise has its own permanent group of customers. Orders are focused on the design and manufacture of a certain class of LSI [6].

Within the framework of this work, a basic set of LSIs for digital signal processing is considered.

At the initial stage of designing such LSIs, the logical and circuitry basis for their construction is determined, typical standard binary elements (NAND, NOR, flip-flops, etc.) are introduced, their design is carried out at various hierarchical levels, and this library is constantly updated. Next, based on standard standard elements, the basic elements of dual-purpose CMOS LSI DSP are designed, which are large, complete functional blocks (RAM, decoders, counters, registers, ALUs, etc.), which are also worked out at all levels of the design process , and they are the basis for the creation of CMOS LSI DSP [7].

With this approach, the design process can be divided between an enterprise focused on the design of basic elements, and the final design of the LSI is carried out by another enterprise.

In this case, at the first stage of design, workstations on inexpensive popular personal computers can be used, which at the same time have sufficient performance to solve the problems of designing basic LSI elements. On the other hand, the mathematical support for designing basic LSI elements is not subject to strict requirements in terms of maximum complexity (number of elements) and speed of calculations.

Thus, in this case, it is possible to “bring closer” computing tools to any developer due to the reasonable cost of both hardware and software problem-oriented tools, the small size of the workstation and ease of operation.

However, as the analysis showed, the most popular workstations on personal computers have significant disadvantages:

– do not have a complete set of problem-oriented programs to implement all stages of the design process;

– the issues of automating the transformation of the circuit structure when moving to another level of modeling have not been sufficiently worked out, which significantly complicates the organization of the end-to-end design cycle and requires the development of their linguistic and information support.

Therefore, the task of creating software that ensures the unity and continuity of a multi-level design process with a single database for implementing an end-to-end design cycle with direct access to local databases, as well as solving all the necessary tasks for

describing, entering, processing and documenting basic projects elements and their characteristics based on the most natural forms of their representation is relevant.

Analysis of the entire list of tasks in the process of multi-level modeling allows us to determine the main functions of linguistic and information support [8, 9]:

– generation of data on typical circuit elements and their structure, setting external influences (including radiation) using graphical methods of description at any hierarchical design level in the form of a single database;
– effective editing of graphic and symbolic information in interactive mode;
– transformation of the circuit structure at various stages of the design process;
– generation of data on the structure of the circuit and its elements for various stages of design;
– graphical interpretation of design results combined with a geometric model of the design object both in the mode of saving the results and displaying them on a graphic monitor directly during the modeling process;
– documentation of the geometric model of the circuit design and modeling results.

At the same time, as shown by the analysis of the current state of LSI modeling tools at various hierarchical levels of the design process, their significant development is required in terms of the creation and inclusion of mathematical support for modeling tools taking into account the radiation effects of static and dynamic logical characteristics of the basic elements of CMOS LSI functional-logical analysis, generation of tests, search for defects.

2 Materials and Methods

Recently, LSIs based on CMOS devices are increasingly used due to a number of advantages compared to LSIs based on bipolar elements. They have a simpler design and manufacturing technology, the ability to operate without static power consumption, higher integration, lower cost, high noise immunity and yield percentage.

Traditionally, it was believed that CMOS LSIs have low resistance to radiation exposure, but modern advances in systems engineering and design and technological techniques have eliminated this drawback, and CMOS LSIs are now widely used in dual-use equipment.

The task of creating a dual-use CMOS LSI requires solving a whole complex of issues related to theoretical and experimental studies of the behavior of standard CMOS LSI elements for pulsed (neutron, gamma radiation, X-ray) and static (gamma radiation, neutron, proton and electronic) types of radiation exposure [10].

At the same time, to design a dual-purpose CMOS LSI, the availability of the entire set of data on the parameters of standard elements at all levels of the design process is required: physical and technological (where the solution of the fundamental system of charge transfer and accumulation equations is required); circuitry (at this level, model parameters are required); functional-logical; behavioral.

To date, the process of research into the creation of radiation-resistant CMOS LSIs has not been completed, and moreover, the state system of standards for the requirements for assessing LSIs for radiation effects has not yet been “settled”. Only relatively recently were additions adopted to the CGS “CLIMATE - 7”, which establishes the composition and parameters of ionizing radiation.

Therefore, the urgent task is to develop tools for modeling the characteristics of the basic elements of dual-use CMOS LSIs.

Moreover, it should be noted that in some cases it is impossible to conduct physical experiments to assess the behavior of elements and LSIs as a whole under conditions of

radiation exposure and, therefore, the only way to predict the behavior of circuits under these conditions is modeling tools.

As part of this work, the task was set to create mathematical models of active elements of CMOS LSIs taking into account radiation effects.

To solve the given problem, it was necessary to test and develop mathematical models of typical CMOS LSI elements taking into account radiation exposure and determine the entire set of necessary parameters and make appropriate changes to the software for modeling static and dynamic characteristics.

At the functional-logical level, modeling of basic elements must solve the problems of logical verification of both serviceable and faulty circuits.

An effective solution to the problem of fault modeling is the basis for a sharp reduction in computational costs in the process of generating test sequences.

The number of faults increases not only due to the increase in the number of circuit elements, but due to the increased packing density of elements on the LSI crystal, the very nature of the faults changes.

Models of constant faults (≡0, ≡1) can no longer fully adequately reflect the many potential errors in the circuit. The high speed of the circuits causes the appearance of logical-dynamic errors represented in the form of parasitic elements at the input of standard elements.

At the same time, taking into account all possible errors will make it impossible to implement the tasks of generating test sequences. Therefore, under these conditions, the influence is limited to the consideration of constant faults, and to simplify the task of constructing tests, methods for constructing testable LSIs and VLSIs are being intensively developed. The scheme can be considered more testable if the procedures for generating tests, their verification and implementation of test diagnostics can be performed subject to compliance with financial and time costs within the established limits.

The testability of logical circuits is ensured by the selection of the appropriate elemental basis and method for constructing logical circuits. Ensuring the testability of designed objects must be addressed already at the initial stages of designing structural elements and standard functional blocks by modeling the characteristics of observability, controllability and testability and excluding “poorly” testable ones from their composition. Improving the “controllability, observability, testability” of a circuit is a simplification for the design object.

Embedded hardware self-testing tools are also being intensively developed [11-13].

In the process of adequate modeling of potential faults in the circuit, the speed of modeling is reduced by an order of magnitude or more. In general, the time required to correct a fault is proportional to N^3, where N is equal to the number of gates in the simulated circuit. To simulate the failure of complex functional blocks using conventional methods, several hours of computer time are spent.

When considering a set of faults as a set of independent random variables, probabilistic and static algorithms are successfully used to solve the test verification problem.

The fault modeling method can be based on the use of the concept of static assessment of controllability parameters and observability of circuit lines. The static fault assessment algorithm uses the results of logic modeling to determine the degree of controllability of each fault and the degree of its observability. That is, based on the simulation results, the probability is calculated that the test vectors will control the fault in question, setting its correspondence to 1 or 0, as well as the probability that the state characterizing this fault will be observed on the vectors.

Such calculations provide, in addition to identifying detected and undetected faults, a measure for assessing the effectiveness of test sequences.

Carrying out preliminary verification of the project at an early stage of development, due to its high speed, allows you to create additional test vectors, eliminate bottlenecks in the digital circuit and prepare for effective and adequate fault modeling.

In this case, a linear dependence of the simulation time on the dimension of the analyzed circuit is achieved. The simulation time is reduced by two orders of magnitude (in comparison with the combined algorithm and guarantees an accuracy of 5-10% completeness assessment with a relatively small increase in the time of logical modeling.

The probabilistic method for determining a test sequence is based on the assumption that the effectiveness of test coverage can be judged by the results of studying the behavior of a circuit with a certain subset of faults $B(f)$, where $B(f) \in F(N)$, $f_n n$, fn nth fault , randomly selected from the entire set of faults $F(N)$ of the set N. The value of the test coverage is estimated using the confidence interval method and it is proved that for large n the inequality holds with probability 0.95

$$| h-p | \leq 0,05,$$

where h=n'/n is the value of test coverage, determined by the usual ratio (n' is the number of detected faults), and p is the probability of extracting the fault under test from the set $F(N)$ randomly. In most cases, such an assessment is quite acceptable when assessing the effectiveness of test coverage. The analysis time depends linearly on the dimension of the analyzed circuit and the use of this technique for a preliminary assessment of an effective test is justified.

However, the efficiency of such estimates is not high enough, and therefore the main efforts should be directed to finding and implementing a way to create input sequences (random or pseudo-random) with a minimum length and a maximum number of detected faults.

Problems of deterministic algorithms (D-algorithm and its varieties) associated with the construction of test sequences for circuits with memory (sequential circuits). In order to apply test analysis methods for combinational circuits to sequential circuits, its functioning is represented as combinational by means of its "unfolding" in time.

However, even in this case, problems arise related to setting the initial state, the upper limit of the number of stages, handling multiple faults, and taking into account faults of the synchronization system.

Due to the fact that a sequential circuit can have several stable states, the problem of ambiguity arises in determining the initial state that gives the fastest solution to the problem. In addition, there is no certainty that such a state exists in a working circuit.

When "unfolding" a circuit in time, there is no unambiguous answer to the question of how many states need to be executed before obtaining a stable state. A large number of iterations significantly increases the computational cost.

Since the test is built for a single fault, when constructing a copy, this fault must be considered as a multiple fault. That is, it is necessary to take special measures to construct a test in order to detect it.

As for the problem of troubleshooting on synchronization paths, then with a certain degree of risk we have to assume that these circuits are error-free and work properly.

Analysis of automated test generation and verification systems shows that problems in such systems are to one degree or another related to minimizing the time of constructing tests, optimizing their parameters and finding rational methods for pseudo-random test generation for sequential circuits.

Thus, the analysis showed that within the framework of the task it is necessary to develop software tools for taking into account controllability, observability, testability of digital circuits and test analysis, ensuring the maximum amount of fault coverage while minimizing computational costs.

3 Research and results

The solution to this problem is the basis for the successful design of any class of microcircuits. It is of particular importance during the transition to submicron technology for the development and production of LSI, VLSI and SoC. In this case, it is necessary to ensure their defect-free design in an acceptable time. Microcircuits with a high degree of integration are practically impossible to design from a “clean sheet” without having a proven library. Therefore, the most important importance was attached to solving the problem of forming and detailed development of libraries of standard elements at all levels of the hierarchical design process.

A methodology for designing standard elements (standard elements are understood as both the simplest logical elements and various functional blocks) of LSI and VLSI is proposed. It is based on a method of rationally combining the intellectual capabilities of a specialist - a circuit designer - and the high productivity of performing labor-intensive routine work on a computer-aided designer's workstation.

To implement this technique, the architecture of an automated workstation based on a personal computer, the structure of building application software, and a method for a unified description of standard elements at all levels of the design process are proposed. Tools have been developed and included in the application software to ensure the development of standard elements at all hierarchical design levels - behavioral, functional-logical, circuitry, topological. The most important distinguishing feature of the developed tools is their versatility, high performance, and the ability to carry out all computational procedures interactively in real time. In addition, several test crystals of standard elements were developed, they were produced, and a method for measuring their static and dynamic parameters was developed. The necessary measurements and tests were carried out, which made it possible to refine the mathematical models of the elements. Using the developed tools and the data obtained from the measurement results of test crystals, a library of standard logical elements and blocks was created, which was the basis for the development and production of fourth and fifth generation microcircuits for the construction of dual-use communication and control systems at base enterprises [14-16].

The transition to submicron technology and the possibility of creating on its basis VLSI and SoC containing millions of elements required a change in both methodology and the development of new design automation tools.

The most important element of the design methodology is the use of reusable SF blocks. This is a key factor in closing the gap between the sophistication of modern semiconductor manufacturing technology and design productivity. The presence of a fairly complete library of SF blocks, tested at all levels of the design process, allows the use of new approaches to the automation of VLSI and SoC design based on them, which ensures a sharp reduction in design time and its error-free performance due to pre-tested solutions (working out SF blocks). In addition, this makes it possible to solve the very labor-intensive task of creating a library of SF blocks in the mode of division of labor between large design DCs and highly specialized enterprises that develop SF blocks. This approach makes it possible to effectively use the intellectual potential of generalists to solve a problem that requires deep knowledge in various fields of science and technology to create equipment and modern microcircuits for its construction.

The decisive contribution to the formation of the scientific and technical infrastructure of the transition of enterprises for the design and production of microelectronic component base, elements and equipment for communication and control systems to a new methodology for design and production in the “system-equipment-chip” mode belongs to the Federal State Unitary Enterprise Research Institute of Microelectronic Equipment “Progress” ", which has been appointed as the lead organization for computer-aided design

of ultra-large-scale integrated circuits in the industry. This organization has developed and implemented a new methodology for the design of highly integrated VLSI and SoC based on the reuse of verified and certified SF blocks; methods of multi-level modeling, synthesis and verification of this class of microcircuits at each design stage: system, functional, logical and physical based on a developed library of SF blocks [17-19].

Tools have been developed for integrating application packages for complex automation of the design of VLSI and dual-use SoCs, characterized by a rational combination of the capabilities of developed and borrowed programs with automated adaptation to the features of the modeling object [20].

4 Conclusion

In the course of the work, requirements for the creation of libraries of SF blocks, which are mandatory for all UREPiSU enterprises, were determined. Only with this approach is it possible to effectively use them within the industry and form a common library of SF blocks on market conditions for collective use. All SF blocks must be accompanied by a full set of their models, documentation, etc., in accordance with the requirements of accepted standards. They should be hierarchically organized and classified to support quick retrieval, based on commercial patterns. Meta data about SF blocks (documentary information that supports quick identification, search and evaluation) should be organized into databases with the ability to quickly search. This library should support various VLSI and SoC design methods (primarily the most common - block and platform design methods).

The use of these methods and tools has significantly reduced development time by eliminating repeated design iterations and ensured the achievement of the required “hard” parameters of the developed microcircuits in terms of power consumption, speed, noise immunity and reliability.

The principles of constructing VLSI CAD Centers are proposed, which form the basis for the creation of DCs of base enterprises and a unified CAD hardware and software complex for the design of a highly integrated element base and radio-electronic equipment.

The work carried out made it possible to develop and organize production at domestic enterprises of modern fifth- and sixth-generation VLSI systems for the construction of equipment for communication and control systems for military and civil purposes.

Thus, a scientific and industrial infrastructure has been created for the development of VLSI and SoC in the industry and its transition to deep submicron technology.

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